Low-Noise Pseudomorphic Dual-Gate Cascode HEMT's with Extremely High Gain

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Abstract— **Quarter micron InGaAs–GaAs dual-gate HEMT's connected as a cascode MMIC in a compact manner have been fabricated and investigated. The devices show a high-output impedance and a very low-feedback capacitance resulting in a high-voltage gain factor g_m/g_d of 125 and a C_{gs}/C_{gd} ratio of 45. The current gain cutoff frequency f_T is 45 GHz and the maximum stable gain is 23.5 dB at 10 GHz and 19 dB at 20 GHz. The pseudomorphic cascode HEMT's show a low-noise figure of 1.1 dB with an associated gain of 22 dB at 10 GHz, at 18 GHz the minimum noise figure is 1.9 dB with 16-dB gain. These data represent the highest gain values and the best noise performance yet reported for dual-gate HEMT devices.**

I. Introduction

DUAL-GATE devices in MESFET and HEMT technology are very advantageous for many applications in high-performance microwave circuits such as variable gain control stages in low-noise and power amplifiers [1]–[3], mixers [4], phase shifters [5], and switches [6]. Especially, HEMT's have proven to be very suitable up to the millimeter-wave region due to their higher current and power gain cutoff frequencies and a lower noise level than MESFET's. In comparison to single-gate (SG) devices, dual-gate (DG) elements connected as a cascode circuit show some additional advantages like higher RF power gain, higher output impedance, and a drastically reduced feedback capacitance. The cascode configuration has been widely described in literature and the suitability of a cascode connection of two SG-HEMT's has been successfully demonstrated in different circuit applications [7], [8].

In this letter, InGaAs–GaAs dual-gate HEMT's are presented whereby the second-gate electrode is internally RF-grounded via two parallel MIM capacitors resulting in a compact cascode unit with the outer dimensions of a single-gate transistor. The fabrication is described and the results of microwave and noise measurements will be given. Extremely high-gain values at simultaneously low-noise levels have been obtained at microwave frequencies making these devices very favorable for gain controllable amplifiers.

II. Fabrication

The pseudomorphic layer structure is grown on 2″ wafers by using MBE on semiinsulating GaAs-substrate. A 100-nm thick GaAs buffer layer and a superlattice consisting of AlAs and GaAs with a thickness of 20 Å each is grown followed by an undoped GaAs layer with a thickness of 7500 Å. The active layer consists of 120 Å undoped InGaAs with an In mole fraction of 21%. The AlGaAs layer with a silicon doping density of $3*10^{18}$ cm^{-3} is separated from the active layer by two thin undoped GaAs and AlGaAs spacers. The structure is completed by a highly *n*-doped GaAs caplayer.

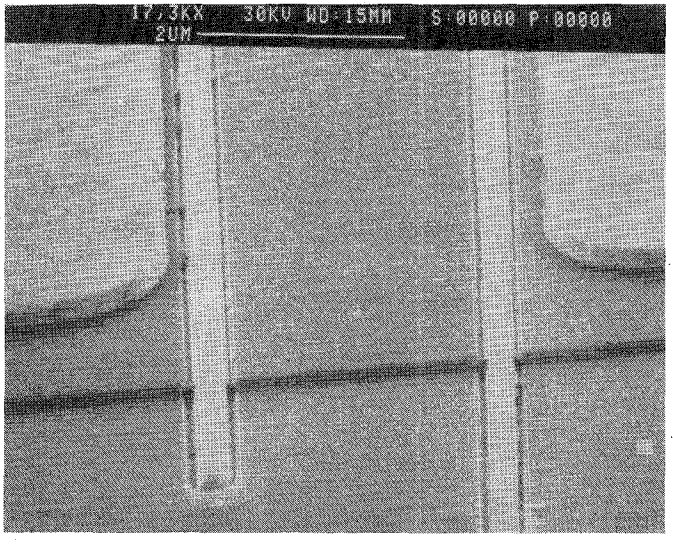

Fig. 1. SEM photograph of the channel region of a 0.25-μm dual-gate HEMT (source on left, drain on right).

The devices are fabricated using a technology that has been established for low-noise monolithic integrated circuits. The active area of the devices is defined by a wet chemical etch step before the ohmic contacts are formed by using a rapid annealed Ge–Ni–Au metallization. The gates and the bottom electrode of the metal-insulator-metal (MIM) capacitors are fabricated using a triple layer process. The lithography step defining the gate pattern is performed by *e*-beam direct writing, the subsequent etching is done by RIE. A 4000-Å- thick Ti–Pt–Au metallization is evaporated resulting in quarter micron gates with a triangular shaped cross-section. The spacing between the first and the second gate is 2.8 μm, the distances from source to gate and from the second gate to the drain contact are 0.2 μm and 0.3 μm, respectively (Fig. 1). Afterwards a Si_3N_4 layer with a capacitance per area of 330 pF/mm^2 is deposited which serves as a passivation layer for the surface and as a dielectric for the MIM capacitors. In the following, the passivation layer and the resist for the air-bridges are patterned

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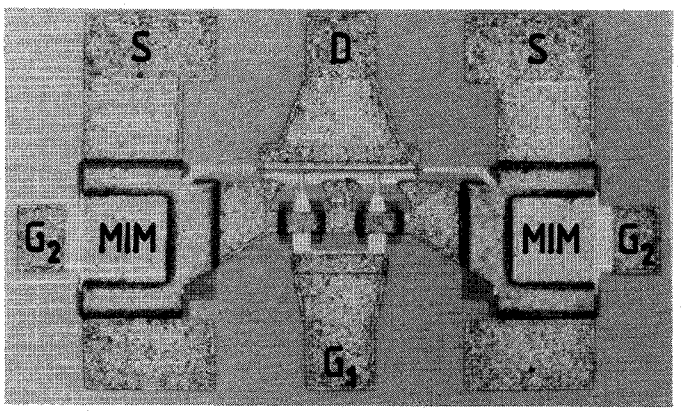
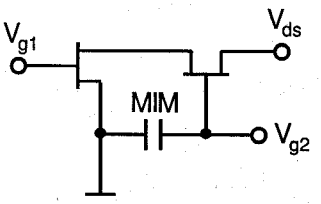


(a)



(b)

Fig. 2. Dual-gate cascode HEMT. (a) Chip photograph ($W_g = 140$ μm, outer dimensions $= 580*335$ μm^2). (b) Schematic diagram of the cascode connection.

before the top metallization is fabricated.

III. DC, Microwave, and Noise Performance

Fig. 2(a) shows a photograph of a dual-gate cascode (DGC-) HEMT with an outer pad configuration designed for on-wafer tests with coplanar G-S-G probe tips. For the first gate a pi-structure was chosen, the second gate is connected to the bottom metallization of the two MIM capacitors located under the source contact pads (Fig. 2(b)). Each capacitor has a nominal value of 2 pF. The additional bias for adjusting the second gate voltage can be applied to a contact pad belonging to the MIM capacitor's bottom electrode. The width of the gates is $4*35$ μm and $4*50$ μm for different devices. From dc measurements the transconductance of the DG-PHEMT's has been determined to be 600 mS/mm. The RF performance of the devices has been measured by using a HP 8510 B vector network analyzer and an on-wafer probe station. The measured S-parameters show a low-output conductance g_d in the order of 1 mS and a small value of the magnitude of $S12$ (mag$S12 < 0.03$) indicating a very low-feedback capacitance. From an equivalent circuit, a high value for the input capacitance to feedback capacitance C_{gs}/C_{gd} ratio of 45 and a very high-voltage gain factor g_m/g_d of 125 has been evaluated. At a second gate voltage of 0.6 V extremely high-insertion gain values of 10.6 dB and 7.5 dB can be measured at

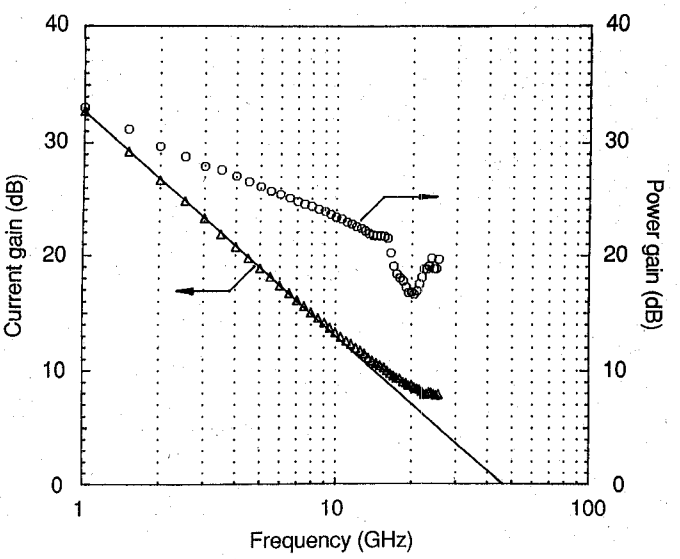


Fig. 3. Measured current-gain and power-gain values versus frequency for a quarter micron dual-gate cascode HEMT ($W_g = 200$ μm) tuned for maximum gain with $V_{g2} = 0.6$ V, $V_{ds} = 2.5$ V, and $I_{ds} = 45.5$ mA.

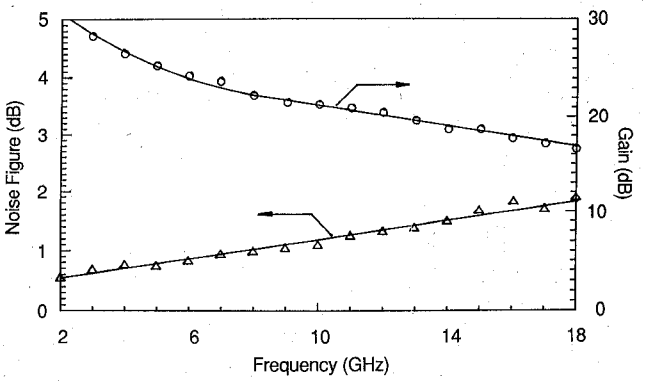


Fig. 4. Minimum noise figure and associated gain versus frequency for a dual-gate cascode HEMT ($W_g = 200$ μm) at 50% I_{dss} ($V_{g2} = 0.6$ V, $V_{ds} = 2.5$ V, and $I_{ds} = 22.5$ mA).

18 GHz and 26 GHz, respectively. From the S parameters, the current gain $h21$, the maximum stable gain, and the maximum available gain have been calculated (Fig. 3). The unity current-gain frequency is 45 GHz, the maximum stable gain is 23.5 dB at 10 GHz and drops to 21.5 dB at 16 GHz. Devices with a gate width of 140 μm show a stable gain of at least 19 dB up to 20 GHz. These gain values are about 5 dB higher than the data reported in [9] and even higher than data obtained with InP-based dual-gate TEGFET's [10]. They represent the highest values yet published for DG-HEMT devices. The maximum frequency of oscillation should be at least 80 GHz according to a MAG frequency roll-off of –12 dB/octave that can be expected from theoretical considerations [11].

On-wafer noise parameter measurements have been performed in the frequency range from 2 GHz to 18 GHz by using a Cascade Microtech NPT 18 noise parameter test set. Fig. 4 shows the minimum noise figure and the associated gain of a DGC-PHEMT with a gate width of 200 μm at 50% I_{dss}. A very low-noise figure of 1.1 dB has been obtained at X-band frequencies with $G_{ass} = 22$ dB. At 18 GHz the

noise figure increases to 1.9 dB at an associated gain of 16 dB. To our knowledge, there are no published data for the noise characteristics of DG-HEMT's, for DG-MESFET's a minimum noise figure of 1.58 dB at 18.54 dB gain has been reported [12]. Single-gate PHEMT's exhibit noise levels as low as 0.5 dB with gain values of about 16 dB [13]. Concerning gain and noise figure the dual-gate cascode devices investigated in this work show state-of-the-art performance.

IV. Conclusion

Quarter micron cascode connected dual-gate HEMT's have been fabricated using a technology developed for monolithic integrated circuits. Extremely high-gain values exceeding 20 dB at simultaneously low-noise levels can be obtained from X-band up to K-band frequencies by using pseudomorphic InGaAs–GaAs material. Therefore, these devices are very favorable candidates for gain controllable stages in low-noise systems.

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